GPLB5X Development Board User Manual

V1.1 - Oct 17, 2008

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0 TABLE OF CONTENT

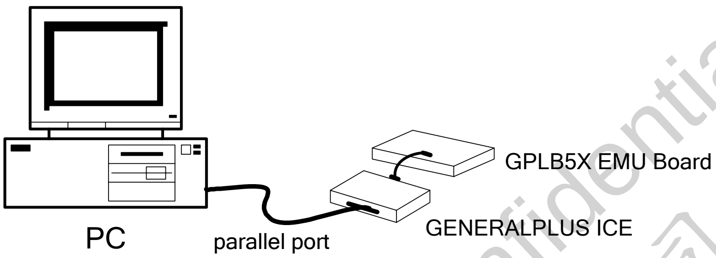
1 REVISION HISTORY

Revision	Date	By	Remark
V1.1	Oct 17, 2008	Frank Kung	Add execute internal ROM notice.
V1.0	July 11, 2008	Frank Kung	Original

2 INTRODUCTION

2.1 Hardware Architecture

The GPLB5X EMU Board is a shared board for GPLB52001A and GPLB52640A. Programmer can easily emulate these devices on board. Simply apply the following connection to start developing your project. Make sure power is properly supplied to both ICE and EMU board.



A hardware overview of GPLB3X development system

2.2 GPLB5X Development Component List

Hardware

1. GPLB5X EMU board
2. Parallel connector (connects ICE & GPLB5X EMU board)
3. GENERALPLUS ICE (In-Circuit Emulator; sold separately)
4. Parallel port (connects to your personal computer; not included in the development kit)
5. Power supplier or adapter with 5V output (not included in the development kit)

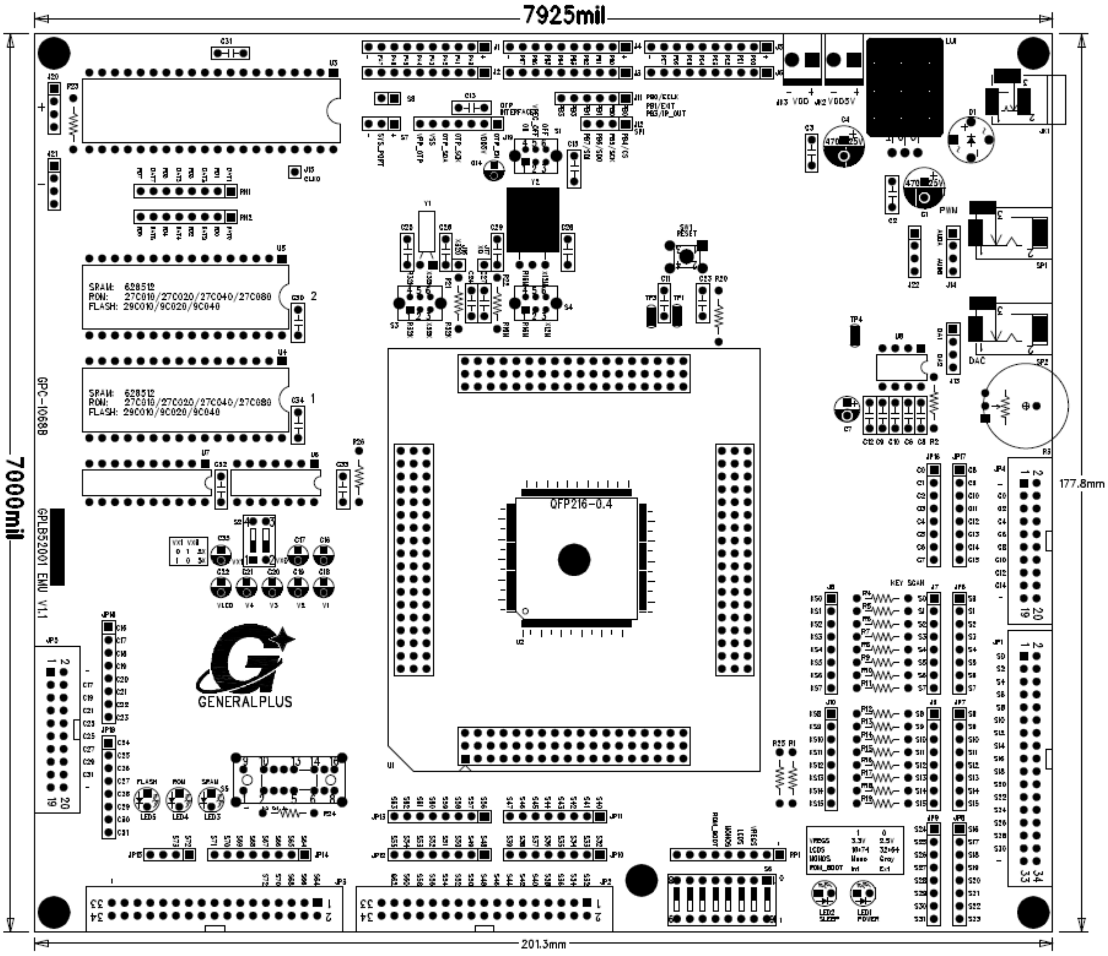
Software

1. FortisIDE software tool. (version 3.0.2)

3 EMU BOARD

3.1 GPLB5X EMU Board V1.1

EMU chip: GPLB52001



Settings Description:

S1: VREG_OFF switch

Name	ON	OFF	Function
VREG_OFF	Enable Power Regulator	Disable Power Regulator	Core power If set disabled, use external power for core power.

S2: **Fixed and don't change**

S3: **32768Hz selector**

Name	VCC	GND	Function
32768Hz Selection	R32K	X32K	32768Hz source selection

S4: **System clock selector**

Name	VCC	GND	Function
Sys_CLK	X12M (12MHz X'TAL)	X16M (ROSC)	System Clock Select

S5: **Memory Selector (SRAM/ROM/FLASH)**

LED3: **SRAM LED**

LED4: **ROM LED**

LED5: **FLASH LED**

S6:

SW Number	Name	SHORT	OPEN	Description
1	--			N/A
2	VREGS	3.3V		Power Regulator Selector (fix to 3.3V)
3	LCDS	16 x 74	32 x 64	LCD dot size selector
4	MONOS	MONO	GRAY	LCD display mode selector
5	ROM_BOOT	INTERNAL	EXTERNAL	ROM Boot
6	--			N/A
7	--			N/A
8	--			N/A

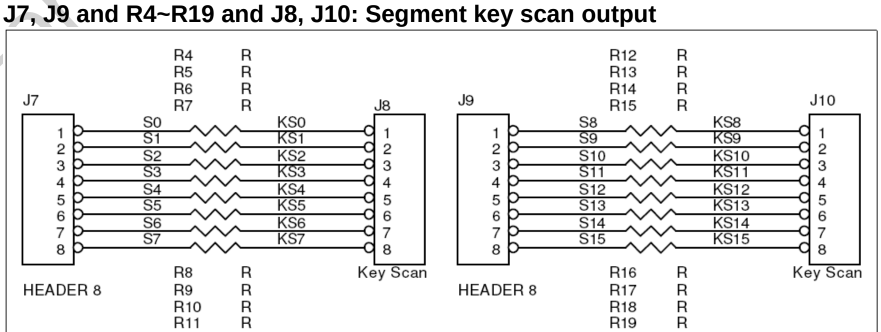
S7: OPEN

S8: Fixed and don't change

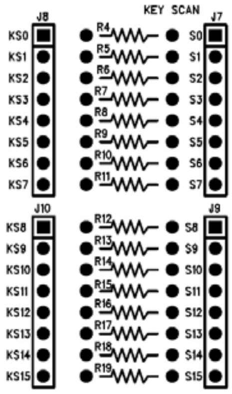
SW1: RESET Switch

JP1~JP19: Common and segment socket

J7, J9 and R4~R19 and J8, J10: Segment key scan output



Key Scan

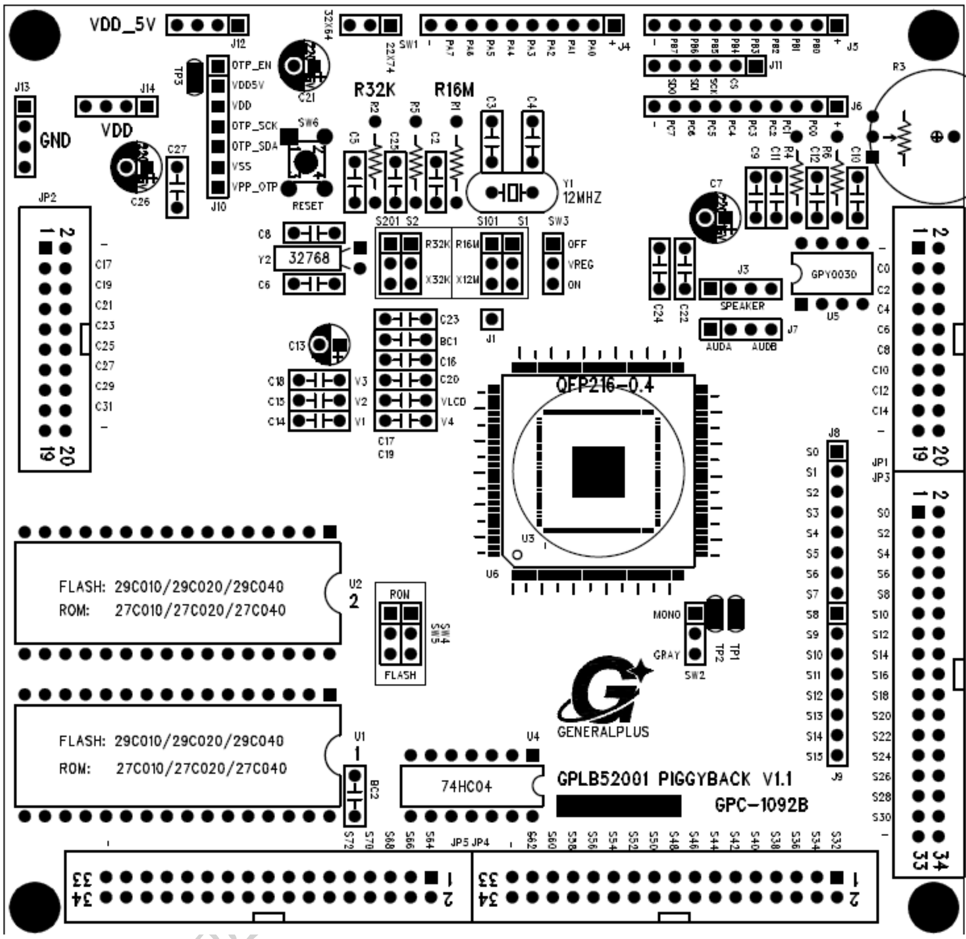


J1, J2:	PortA
J3, J4:	PortB
J5, J6:	PortC
J11:	ECLK, EXTI, IR Output connecter
J12:	SPI interface
JK1:	Adapter input (9V)
JK2:	General power input (5V)
J20:	General power input (5V)
JK3:	3.3V VDD power Input
J21:	GND connecter
LED1:	Power LED (ON when powered on)
LED2:	Sleep LED (ON while sleeping)
LED3:	RAM LED (ON when switch S5 to RAM)
LED4:	ROM LED (ON when switch S5 to ROM)
LED5:	FLASH LED (ON when switch S5 to FLASH)
R22:	System clock resistor (ROSC)
R21:	R32K resistor
Y2:	12MHz X'TAL for System Clock
Y1:	32768Hz X'TAL
U1, U2:	GPLB52001 Chip
U3:	CPU socket for ICE used
U4, U5:	RAM / ROM / FLASH, dependent on S5
U8:	GPY0030 OP-AMP
SP1:	PWM outputs speaker
J14, J22:	PWM output connector
SP2:	DAC output Speaker
J13:	DAC output connecter

4 PIGGYBACK

4.1 GPLB5X Piggyback V1.1

EMU chip: GPLB52001



Settings Description

S101: System clock selector

Name	VCC	GND	Function
Sys_CLK	X12M (12MHz X'TAL)	X16M (ROSC)	System Clock Select

S1: X12M / R16M selector

S201: 32768Hz selector

Name	VCC	GND	Function
32768Hz Selection	R32K	X32K	32768Hz source selection

S2: X32K / R32K selector

SW1: LCD dot size selector

Name	VCC	GND	Function
LCDS	22 x 74	32 x 64	LCD display mode selection

SW2: LCD display mode selector

Name	VCC	GND	Function
MONOS	MONO	Gray	LCD display mode selection

SW3: VREG_OFF switch

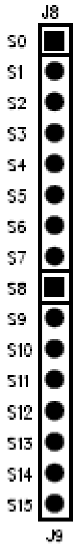
Name	VCC	GND	Function
VREG_OFF	Disable Power Regulator	Enable Power Regulator	LCD Charge Pump control

SW4, SW5: Flash / ROM selector

SW6: RESET Switch

JP1~JP5: Common and segment socket

J8, J9: Segment key scan output



J1:	Open
J3:	DAC output connecter
J4:	PortA
J5:	PortB
J6:	PortC
J7:	PWM output connector
J11:	SPI interface
J12:	General power input (5V)
J13:	GND connecter
J14:	3.3V VDD power Input

R1:	System clock resistor (ROSC)
R2:	R32K resistor
Y1:	12MHz X'TAL for System Clock
Y2:	32768Hz X'TAL

U1, U2:	ROM / FLASH, dependent on SW4 & SW5
U3, U6:	GPLB52001 Chip
U5:	GPY0030 OP-AMP

5 GPLB52001A OTP SERIAL PROGRAMMING INTERFACE

5.1 Serial Interface at Serial Programming Mode

5.1.1 GPLB52001A uses serial interface to program/read OTP through OTP_SCK and OTP_SDA

5.1.2 Apply OTP_ENABLE to VDD to enable serial OTP programming interface

OTP_ENABLE	Mode
0	Normal mode
1	Serial programming mode

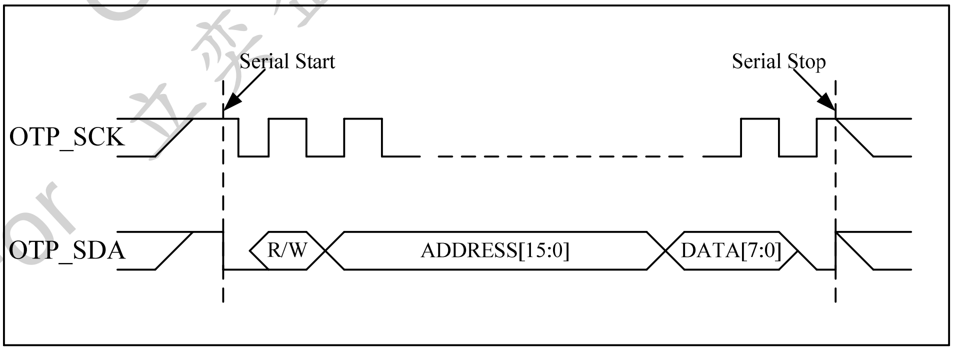
Table 1, OTP Mode Selection

5.1.3 Use pin for programming of GPLB52001A

Pin name	Function name of Programming mode	Function
VDD	VDD	3.3V
VPP	VPP	7.5V
OTP_SDA/ XINT	SDATA	Bi-Directional Data
OTP_SCK/ XMI	SCLK	Clock
OTP_ENABLE	0 or 1 selected	Mode control
Test	Test*	Test mode selection (connect to VSS)

Note*: Test pin can use as floating because it has pull-low in internal.

5.1.4 Serial interface data format



Note:

1. Except Start/Stop bit, OTP_SDA should remain unchanged while OTP_SCK is high.
2. R/W bit: “0” for serial write, “1” for serial read.
3. ADDRESS Range: $0000h ~ FFFFFh: User program’s area.

5.1.5 Security bit (CPU View: $CBB0 fill “00H”)

A security bit is implemented for code protection. If security bit is enabled, it will set OTP to secure mode which means OTP is not writable and all data read from OTP will be ‘00h’.

Security bit	Function
Enable	Security mode
Disable	Normal mode

5.2 Using Generalplus Writer Tool to Program OTP ROM Data

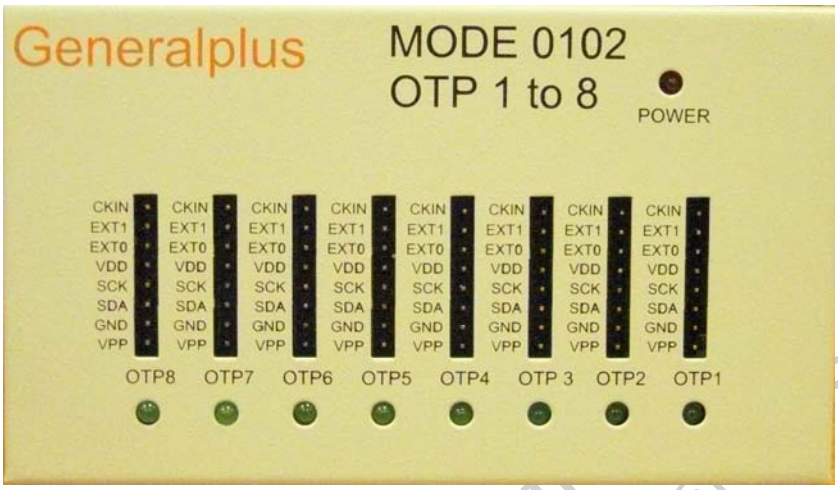
The GPLB52001A OTP Writer system includes a Main Board and a Multi-Programming Adaptor.

Main Board (OTP-W-22-M0):



Multi-Programming Adaptor (OTP-W-22-M0102):

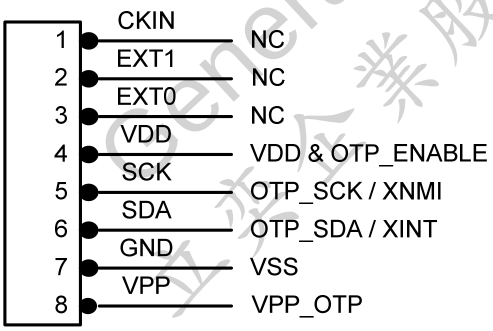
To program GPL52001A in user's system board, a Multi-Programming Adaptor must be used, allowing up to 8 OTPs to be programmed at a time.



5.3 Serial Programming Connect Port

It can use extra connector on Multi-Programming Adaptor to connect the product.

5.3.1 The Connect port on Multi-Progamming Adaptor



OTP 1 to 8 Board Connect

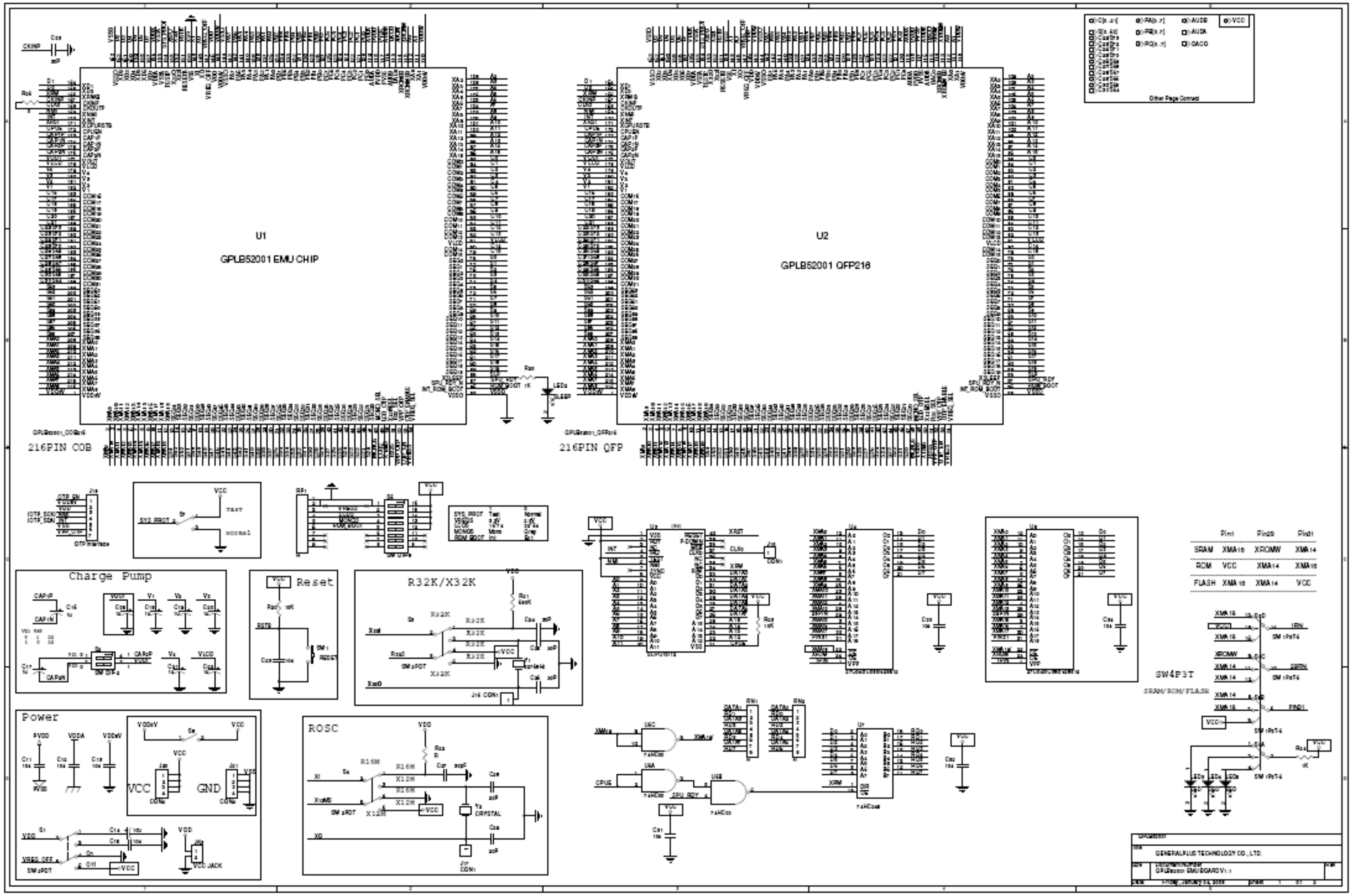
ALL Writer Serial Pin	GPLB52001A PAD
VDD	VDD, VDD5V, PVDD, VDDA & OTP_ENABLE
SCK	OTP_SCK / XNMI
SDA	OTP_SDA / XINT
GND	VSS, VSSO, PVSS & VSSA
VPP	VPP_OTP

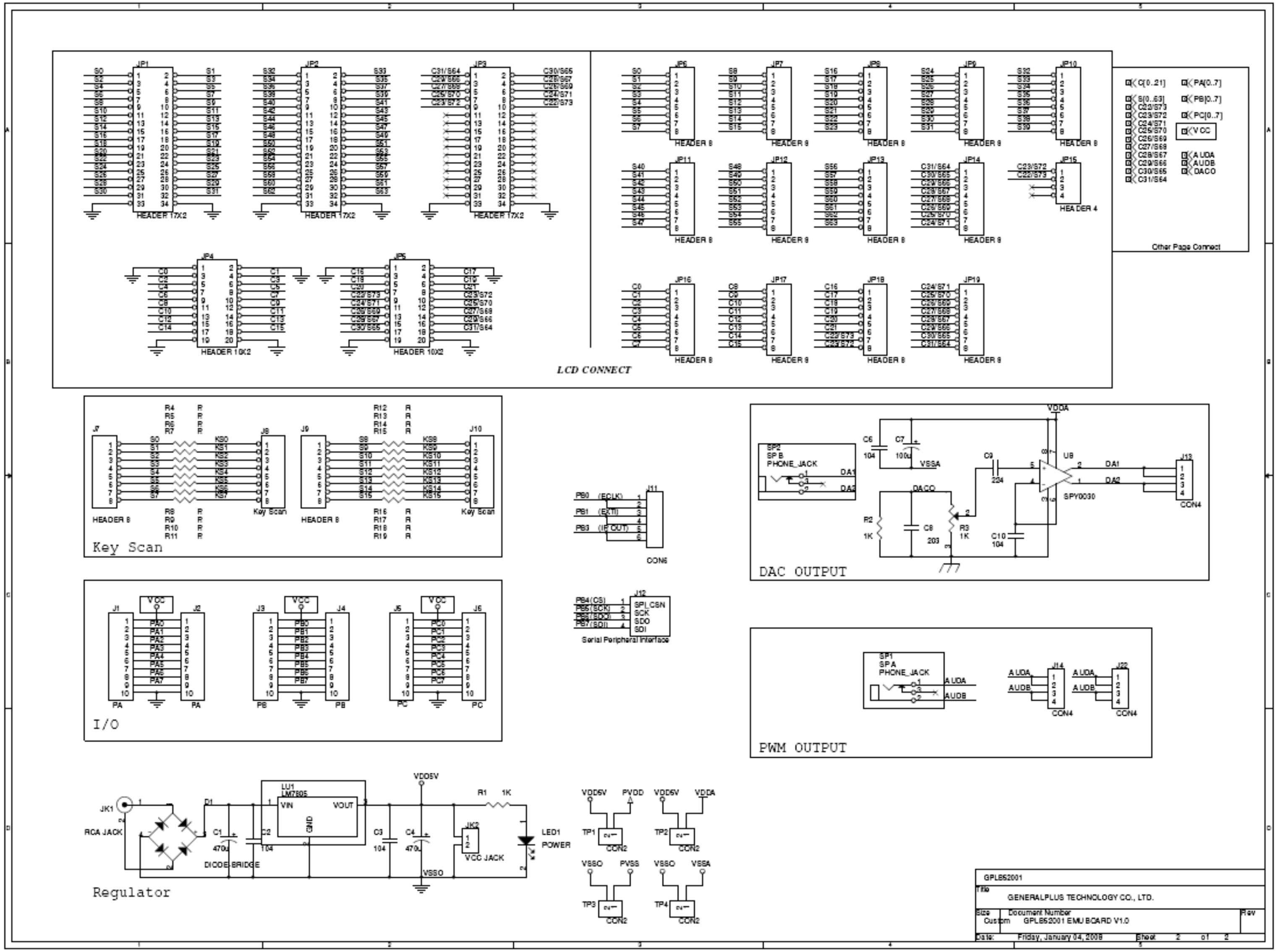
5.4 Notes to Executing Internal ROM

Please pay extra attention the following pins when user finishes programming and wants to boot from internal ROM.

GPLB52001A PAD	Connect to
CKINP	CKOUTP
CPUEN	VDD5V
INT_ROM_BOOT	VDD5V
SPU_RDY_N	Floating

6 APPENDIX A: GPLB5X EMU BOARD SCHEMATICS




LCD CONNECT
Key Scan
I/O
DAC OUTPUT
PWM OUTPUT
Regulator
Other Page Connect
Serial Peripheral Interface
GPLB52001
GENERALPLUS TECHNOLOGY CO., LTD.
Document Number
GPLB52001 EMU BOARD V1.0
Friday, January 04, 2008

7 APPENDIX B: GPLB5X PIGGYBACK SCHEMATICS

